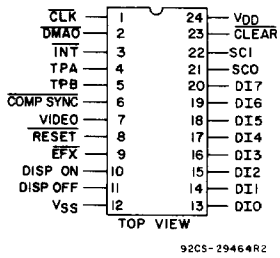
CDP1861C

Preliminary Data

Video Display Controller



TERMINAL ASSIGNMENT

Features:

- *Supports bit-mapped video display for graphic flexibility*
- *Generates composite horizontal and vertical sync*
- *Programmable vertical resolution for matrix display of up to 64 x 128 segments*
- *Real-time interrupt generator*
- *Clear input*
- *External display control*

The RCA-CDP1861C is a video display controller designed for use in CDP1800-series microprocessor systems.

The CDP1861C utilizes many of the features of the CDP1800-series microprocessor to simplify control and minimize the need for external components. The DMA feature of the CDP1800-series microprocessor may be used for direct data transfers from memory to the CDP1861C. The INTERRUPT input and the I/O command lines may be used to perform the necessary handshaking between the CDP1800-series microprocessor and the CDP1861C. Timing may be simplified by operating the microprocessor at a clock frequency of 1.76064-MHz (the standard color frequency of 3.58 MHz, divided by 2, may also be used in some applications). The clock and the CDP1800-series microprocessor timing signals (TPA and TPB) may then be used to set the interface timing (as shown in the system diagram). In general, the clock frequency equals the number of fields per second (60), times the number of lines per field (262), times the number of machine cycles per line (14), times the number of bits per byte (8). In DMA operation, each machine cycle is a memory access.

Flexibility in vertical resolution may be obtained by synchronizing the CDP1861C with the CDP1800-series microprocessor and employing direct program control over the DMA process in real time. The actual video display takes place during a "window" of 4.6 milliseconds out of each 16.7-millisecond TV field. Throughout each such display window, a CDP1800-series microprocessor interrupt program may be used to manipulate the DMA pointer, re-issuing a given line of the display several times to save memory storage at the expense of reduced vertical resolution.

The CDP1861C generates composite vertical and horizontal sync plus luminance signals which can be combined externally to create an NTSC compatible composite video signal. This composite vertical and horizontal sync output signal ($\overline{\text{COMP SYNC}}$) is generated from the sync reference (TPA) and TBP inputs. Vertical sync is derived from horizontal sync by dividing the horizontal sync frequency by 262. The composite sync signal generates timing for a non-interlace video display of 262 lines per field.

The CDP1861C generates an interrupt request ($\overline{\text{INT}}$) once per field, 62 lines after the trailing edge of vertical sync and two line before the raster has reached a "display window" (see Fig. 5). This request alerts the CDP1800-series microprocessor (or other control system) to prepare for DMA (direct memory access) activity. The CDP1861C DISP STATUS (EFX) output goes low during the 4 lines before the display window, and again during the last 4 lines of the window. This signal may be used to give early warning of the display window and to release the control system from monitoring the DMA activity.

Beginning in the third machine cycle of each line of the display window, and lasting for 8 cycles, the CDP1861C asserts the $\overline{\text{DMA0}}$ output to request a sequency of eight 8-bit bytes, which are then used to generate the VIDEO signal. Then, when control signals SCI and SCO are low and high respectively, each assertion of the TPB input causes the CDP1861C to read a byte from the BUS lines, and immediately to shift it out on the VIDEO output, high-order bit first. A DMA pointer defines an area of memory which is accessed by the CDP1861C to provide a bit-mapped display.

The display on (DISP ON) and display off (DISP OFF) inputs set and reset an internal control flip-flop in the CDP1861C. When this flip-flop is set, $\overline{\text{DMAO}}$ and $\overline{\text{INT}}$ are enabled; when reset, they are disabled.

The reset input ($\overline{\text{RESET}}$) is a Schmitt trigger input that resets the CDP1861C. The $\overline{\text{CLEAR}}$ output is a conditioned output pulse which can be used to reset the external system.

The CDP1861C is supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) ..... -0.5 to +7 V
(Voltage referenced to V_{SS} Terminal)
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS, at T_A = -40 to +85°C, Except as Noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
					CDP1861CD CDP1861CE			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN.	TYP.*	MAX.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	50	250	μA
Input Leakage Current,	I_{IN}	Any Input	0, 5	5	—	±0.1	±1	μA
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	V
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.05	V
Output Voltage High-Level (Except $\overline{DMAO}$, $\overline{INT}$)	V_{OH}	—	0, 5	5	4.95	5	—	
Output Low Drive (Sink) Current	I_{OL}							mA
$\overline{INT}$, $\overline{DMAO}$:		0.4	0, 5	5	0.2	0.5	—	
$\overline{CLEAR}$, $\overline{EF}$:		0.4	0, 5	5	0.4	0.8	—	
VIDEO, $\overline{COMP\ SYNC}$:		0.4	0, 5	5	0.8	1.6	—	
Output High Drive (Source) Current	I_{OH}							mA
$\overline{CLEAR}$ $\overline{EF}$:		4.6	0, 5	5	-0.4	-0.8	—	
VIDEO, $\overline{COMP\ SYNC}$:		4.6	0, 5	5	-0.5	-1	—	
RESET (Schmitt Trig.)								V
Pos. Trig. Threshold	V_P	—	—	5	—	2.5	—	
Neg. Trig. Threshold	V_N	—	—	5	—	1.7	—	
Hysteresis Voltage	V_H	—	—	5	—	0.8	—	

* Typical values are for T_A = 25°C.

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		CONDITIONS	LIMITS		UNITS
			CDP1861C		
		V_{DD} (V)	MIN.	MAX.	
DC Operating Voltage Range		—	4	6.5	V
Input Voltage Range		—	V_{SS}	V_{DD}	
Maximum Input Rise or Fall Time	t_r, t_f	5	—	5	μs
Maximum Clock Input Frequency	f_{CL}	5	DC	2.5	MHz

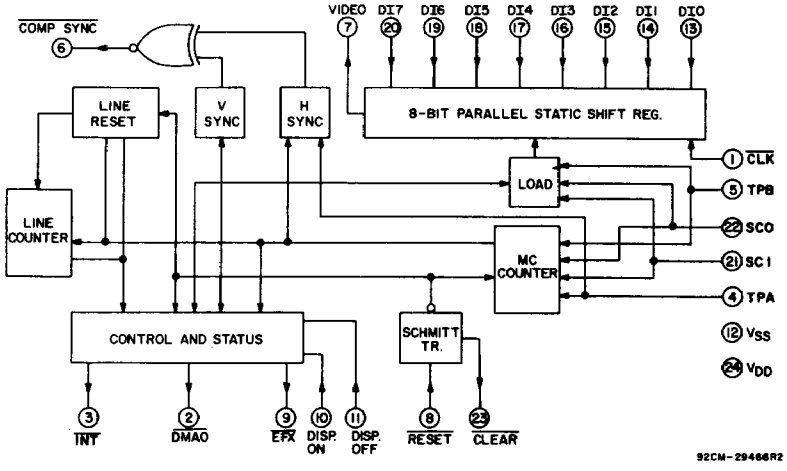


Fig. 1 - CDP1861C block diagram.

FUNCTIONAL DESCRIPTION OF CDP1861C TERMINALS

$\overline{CLK}$:

The active low input for an externally generated single-phase clock which determines the clock rate for the 8-bit data shift register. Data are shifted on the high-to-low transition of the $\overline{CLK}$ input signal, most significant bit first. A low level (V_{SS}) is shifted into the least significant bit.

The $\overline{CLK}$ signal may be derived directly from the CDP1800-series microprocessor by connecting the $\overline{CLK}$ terminal of the CDP1861C to the $\overline{XTAL}$ terminal of the CDP1800-series microprocessor.

$\overline{DMAO}$:

An active low output (V_{SS}) that requests an 8-bit data transfer. The output signal is from the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD}. Depending on the status of the SC0 and SC1 input signals at horizontal sync time, DMA requests are initiated on the leading edge of the second TPA input signal following the horizontal sync output. This feature is necessary in order to reference the data requests to the program's ability to respond to them, insuring that data will always be initiated at the same point on the display. The system should respond to a $\overline{DMAO}$ by setting SC0 high (V_{DD}), and SC1 low (V_{SS}), permitting data transfer. Data will be loaded on the subsequent 8 TPB input signals.

$\overline{DMAO}$ will be terminated on the ninth sync pulse, at which time SC0 should be set low (V_{SS}) prior to the next TPB command. Timing is illustrated in Figs. 3 and 5. The $\overline{DMAO}$ output signal may be connected to the $\overline{DMA\ OUT}$ Terminal of the CDP1800-series microprocessor, which responds as discussed above.

$\overline{INT}$:

An active low (V_{SS}) output signal two horizontal cycles prior to the display, as shown in Figs. 3 and 5. This signal is the output of the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD}. The $\overline{INT}$ output signal is normally connected to the $\overline{INTERRUPT}$ input terminal of the CDP1800-series microprocessor. In a CDP1800-series microprocessor based system, 29 machine cycles occur from initiation of an $\overline{INT}$ until the $\overline{DMAO}$.

TPA:

An active high timing pulse occuring once for every 8 clock pulses. The TPA signal is used as the clock for the horizontal line counter. It is normally tied to the TPA teminal of the CDP1800-series microprocessor. The TPA signal precedes the TPB signal.

TPB:

An active high timing pulse occurring once for every 8 clock pulses. The TPB signal is used as a strobe for gating the output of the counter and for loading data into the data register. It is normally connected to the TPB terminal of the CDP1800-series microprocessor.

$\overline{COMP\ SYNC}$:

An active low output signal resulting from the exclusive "OR" of the output of the horizontal and vertical counters. $\overline{COMP\ SYNC}$ can be combined with the VIDEO output to form a composite video signal.

The $\overline{COMP\ SYNC}$ output frequency and pulse duration are determined by the TPA and TPB input signals. A horizontal sync pulse is initiated by the trailing edge of the TPB input signal following the 13th or 14th TPA input, as determined by the status of the SC0 and SC1 input signals, and is terminated on the leading edge of the subsequent second count of the TPA input.

Vertical timing is generated coincident with the 262nd horizontal timing pulse and is present for six horizontal clock cycles. Idealized timing is illustrated in Figs. 2 and 4.

VIDEO:

An active high output from the most significant bit of the 8-bit P/S data register. It is used to determine the luminance level and may be combined externally with the $\overline{COMP\ SYNC}$ output signal to form a composite video signal.

$\overline{RESET}$:

An active low input signal which initializes the counters, inhibits the display, and places all control outputs in the high (V_{DD}) state. Refer to Fig. 3.

FUNCTIONAL DESCRIPTION OF CDP1861C TERMINALS (Cont'd)

RESET (Cont'd)

The $\overline{\text{RESET}}$ terminal is a Schmitt-trigger-type input which permits the use of an external RC network to provide a power-on reset.

$\overline{\text{EFX}}$:

An active low output signal which occurs for a period of four horizontal cycles prior to the beginning and end of the 128-line display window, as illustrated in Figs. 2 and 4. The signal can be used by the program software routines to indicate the boundaries of the display area. It is normally connected to a CDP1800-series microprocessor $\overline{\text{EF1}}$-$\overline{\text{EF4}}$ FLAG input terminal.

DISP ON, DISP OFF:

Active high input signals that control the display. When enabled by pulsing DISP ON high (V_{DD}), data transfers, DMA, and interrupt requests are permitted. These operations are inhibited by the low-to-high transition of the DISP OFF input signal if DISP ON is low (V_{SS}). The $\overline{\text{RESET}}$ signal also inhibits the display. When inhibited, the internal counters remain operational. Sync and display status signals are generated. Video output becomes low when the register is emptied. Table I indicates the enable/disable conditions.

The DISP ON and DISP OFF signals may be provided by the I/O commands (N bits) of the CDP1800-series microprocessor.

TABLE I

	SIGNAL		
STATE	**$\overline{\text{RESET}}$**	**DISP ON**	**DISP OFF**
RESET	L	L	X
INVALID	L	H	X
DISPLAY ENABLE	H	⎍	X
DISPLAY DISABLE	H	L	⎍

D10 — D17:

Input signals to the data register. Data are loaded during the high-to-low transition of the $\overline{\text{CLK}}$ only when TPB, DISP ON, and SC0 are high (V_{DD}), SC1 is low (V_{SS}), and the CDP1861C is enabled.

The data input signals are normally connected to the 8-bit microprocessor data bus.

SC0, SC1:

Input signals used to synchronize the operation of the CDP1861C will its controller. They should be initiated prior to the TPA input and terminate after the TPB input pulse.

These control signals are sampled at two different times: **1)** During the horizontal sync output when the TPA input is present, the CDP1861C expects to see SC1 = 1 (V_{DD}) and SC0 = 0 (V_{SS}). Any other combination will result in the skipping of one of the normal 14 cycles per line. This feature allows the CDP1800-series microprocessor to force initial instruction fetch/execute sync with the CDP1861C, and assures sync in case it is later lost for any reason. **2)** In the 6 cycles following the CDP1861C $\overline{\text{DMAO}}$ assertion, the CDP1861C expects to see SC1 = 0 and SC0 = 1. Any other combination will prevent the CDP1861C from loading data from the bus.

These signals may be connected to the STATE CODE (SC0, SC1) outputs of the CDP1800-series microprocessor.

$\overline{\text{CLEAR}}$:

The output of the Schmitt trigger (reset input circuitry) provides high speed transitions that may be used to reset other devices. It may be connected to the $\overline{\text{CLEAR}}$ terminal of the CDP1800-series microprocessor.

V_{DD}, V_{SS}:

V_{DD} is the positive supply voltage terminal, V_{SS} is the negative supply voltage terminal and is normally connected to ground.

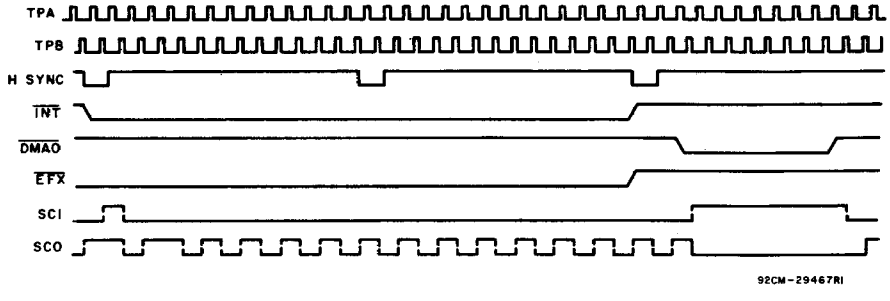


Fig. 2 - Horizontal sync timing diagram.

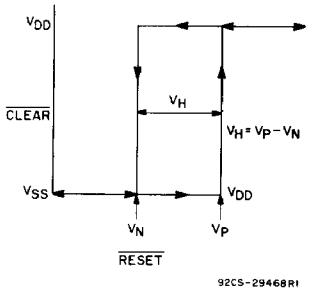


Fig. 3 - Reset transfer characteristics.

APPLICATION INFORMATION (CDP1861C DIRECTLY CONTROLLED BY THE CDP1800-SERIES MICROPROCESSOR)

Figure 5 shows a simple graphic display system using the CDP1800-series microprocessor and the CDP1861C. The CDP1861C uses both the INTERRUPT and direct memory access (DMA) output channel of the microprocessor for display refresh. The microprocessor specifies the area of memory displayed via the interrupt routines, and the DMA output channel is the mechanism which transfers the data from memory to the CDP1861C via the 8-bit data bus. The data are then shifted out one bit at a time at the clock frequency to generate the video (VIDEO) signal.

The composite sync ($\overline{\text{COMP SYNC}}$) signal creates a 262-line-per-field, 60-field-per-second non-interlace video picture. The non-interlaced picture frame for this display consists of two even fields of 262 horizontal lines each. This format differs slightly from the National Television Standard (NTSC) which has a 525-line interlaced picture frame of one odd field and one even field. The vertical sync pulse generated at $\overline{\text{COMP SYNC}}$ of the CDP1861C has no equalizing pulses but is serrated to maintain horizontal synchronization during the vertical blanking time. The VIDEO and $\overline{\text{COMP SYNC}}$ pulses are resistively coupled to create the composite video, which can be supplied directly to a video monitor, a modified TV receiver, or a FCC approved rf modulator.

A clock source of 3.58 MHz, the NTSC color frequency, if divided by 2, may be used for some applications in place of the 1.76-MHz crystal shown in Fig. 5. Deviations from the NTSC frequencies are as follows:

The user should determine which choice of frequencies provides an optimal cost/performance trade-off for his application. Generally, video CRT's are more sensitive to line frequency accuracy than to field frequency accuracy.

The display is a bit map of memory. Each bit in the display memory corresponds to one spot on the video screen. Logical 1 (V_{DD}) bits in memory correspond to white or lighted spots in the display. The highest resolution that may be produced is 128 vertical by 64-horizontal segments. This resolution requires 1024 bytes of memory for the display. The upper left-most spot that can be displayed on the video screen is the most significant bit of the first byte in the display refresh memory buffer. The starting location of the display buffer is initialized in the INTERRUPT routine and may be anywhere in addressable memory (ROM, RAM, or both). The lower right-most spot that can be displayed is the least significant bit of the last byte of the display bit map. For each of the 128 horizontal display lines, 8 bytes of memory are sequentially accessed and displayed from left to right on the video screen. Adjacent illuminated spots appear contiguous both in the horizontal and in the vertical directions. All display manipulations are accomplished by changing the data within the display buffer or by changing display buffers.

To control the CDP1861C as shown in Fig. 5, the CDP1800-series microprocessor must be in synchronization with the CDP1861C during the display window. Exactly six machine cycles must be executed beyond the eight DMA cycles during each line, and an even number of cycles (262 x 14) must be executed from the start of one display window to the start of the next. These requirements insure that the DMA burst will not be delayed one cycle waiting for an instruction to finish — this delay would cause jitter on the screen. These requirements can be accomplished in two steps: **1)** the main program must not execute any 3-cycle instructions (i.e., SKIP, LONG BRANCHES, and NOP), and **2)** the interrupt routine, including the interrupt cycle itself, must employ an even number of cycles, and must be synchronized with the DMA bursts. There must be 29 cycles between the INTERRUPT cycle (S3) and the first burst of eight DMA cycles. This timing is accomplished by executing an early 3-cycle instruction to compensate for the INTERRUPT cycle. Furthermore, exactly three 2-cycle instructions must be executed between each sucessive burst. Occasionally these restrictions may be ignored at the expense of jitter on the screen.

For the 128 x 64 display, the CDP1800-series microprocessor software requirement is straightforward. The DISP STATUS/$\overline{\text{EF1}}$ line is not required, and $\overline{\text{EF1}}$ may be used for other purposes. A simple interrupt routine merely resets the DMA pointer, R0, to the beginning of the display buffer area (see Fig. 8) — note the 3-cycle NOP instruction at the beginning which compensates for the 1-cycle interrupt. The first burst of eight DMA cycles occurs just as this routine finishes, as indicated by the bracket following the RETURN instruction (70). Exactly 29 cycles separate the interrupt request cycle and the first DMA burst. The interrupt routine must last at least 28 cycles, because the interrupt request line is held up that long by the CDP1861C.

When less RAM is to be used (less resolution), a more complicated interrupt routine is used. The interrupt routine is protracted for the full duration of the display window, and the six free cycles in each line are used to execute three instructions, which maintain control over the DMA pointer, R0.1. In the simplest cases, each line of 8 bytes is repeated n times to give 128/n vertical resolution. With n = 4, for example, 64 x 32 resolution is obtained. Such an interrupt routine is shown in Fig. 7. The use of three instructions per

APPLICATION INFORMATION (CDP1861C DIRECTLY CONTROLLED BY THE CDP1800-SERIES MICROPROCESSOR) (Cont'd)

line does not leave time to control a loop, so each of four copies of the line corresponds to three instructions in the main loop, starting at $\overline{EFX}$. The $\overline{EFX}$ signal, applied to $\overline{EF1}$, is used to signal the last pass through the loop.

For other values of n, similar routines can be devised. For n = 2, the 64 x 64 format, the last 4 lines need special treatment (see Fig. 6). Other schemes are possible, resulting in other resolutions which vary on command from the main program, or even resolutions which vary through the display window.

In general, additional functions may be implemented in the routine before returning to the main program. For example, a real-time clock can be maintained by incrementing a counter once on each interrupt, i.e., once per 1/60 second. Another example is vertical "scrolling" of the display, wherein the starting address in a display file is incremented or reincremented at regular intervals.

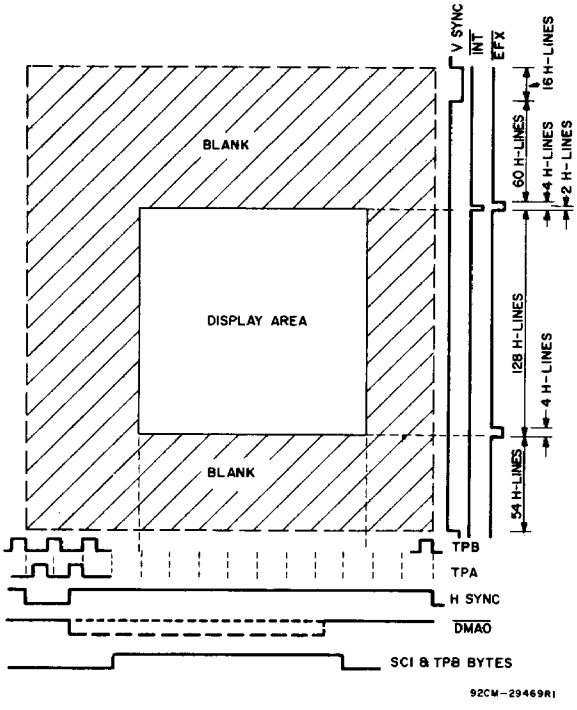


Fig. 4 - Spatial diagram of one video display field (not to scale).

NTSC		CLOCK FREQUENCIES (MHz)		
		1.76064	1.764000	3.579545/2
Line Freq.	15750	15720	15750	15980
Field Freq.	60	60	60.11	60.99

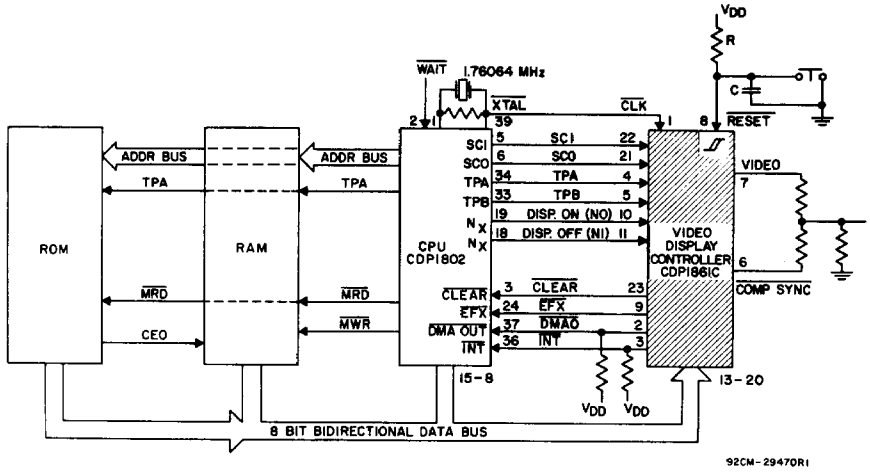


Fig. 5 - Typical CDP1802/CDP1861C video display system.

Machine Code		Assembly Language	Comments
72	INTRET	: LDXA	. . RESTORE D
70		RET	. . RETURN
C4	INT	: NOP	. . 3 CYC. INSTR. FOR PGM. SYNC
22		DEC R2	. . R2 IS STACK PTR
78		SAV	. . T→STACK
22		DEC R2	
52		STR R2	. . D→STACK
F8-B0		A.1 (DISMEM)→RO.1	. . DISMEM IS START ADDR
F8-A0		A.0 (DISMEM)→RO.0	. . OF DISPLAY MEMORY
C4, C4		NOP; NOP	. . NOPS FOR PGM SYNC
E2		SEX2	
80]	DISP	: GLO RO	. . NEW LINE
E2		SEX2	. . NOP
20		DEC RO	. . RESTORES RO.1 IF PASS PG
A0]		PLO RO	. . REPEATS SAME LINE
E2		SEX2	. . NOP
3C—		BN1 DISP	. . LOOP 60 TIMES
80]	DISEF	: GLO RO	. . LAST 4 VIDEO LINES
E2		SEX2	. . NOP
20 A0]		DEC RO; PLO RO	
E2		SEX2	. . NOP
34—		B1 DISEF	
30—		BR INTRET	. . END OF DISPLAY

Fig. 6 - Interrupt routine for 64 x 64 format (2 pgs mem).

Machine Code		Assembly Language	Comments
72	INTRET	: LDXA	. . RESTORE D
70		RET	. . RETURN
C4	INT	: NOP	. . 3 CYC. INSTRU. USED
			. . FOR PGM. SYNC
22		DEC R2	. . R2 IS STACK PTR
78		SAV	. . T→STACK
22		DEC R2	
52		STR R2	. . D→STACK
F8-B0		A.1 (DISMEM)→R0.1	. . LOAD RO WITH
F8-A0		A.0 (DISMEM)→R0.0	. . START ADDR. OF DISP. MEM
C4, C4		NOP; NOP	. . NOPS USED FOR SYNC
E2	DISP	: SEX2	
80]		GLO RO	. . LINE START ADDR.→D
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0]		PLO RO	. . LINE START ADDR.→RO.0
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0]		PLO RO	. . LINE START ADDR.→RO.0
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0]		PLO RO	. . REPEATS SAME LINE
3C—		BN1 DISP	. . LOOPS 32 TIMES
30—		BR INTRET	. . END OF DIPLAY

Fig. 7 - Interrupt routine for 64 x 32 format (1 pg mem).

Machine Code		Assembly Language	Comments
72	INTRET	: LDXA	. . RESTORE D
70]		RET	. . RETURN
C4	INT	: NOP	. . ENTRY POINT
22		DEC R2	. . R2 = STACK PTR
78		SAV	. . T→STACK
22		DEC R2	
52		STR R2	. . D→STACK
E2, E2		SEX R2; SEX R2	. . NOP
F8-B0		A.1 (DISMEM)→RO.1	. . LOAD RO WITH
F8-A0		A.0 (DISMEM)→RO.0	. . START ADDR OF DISP. MEM.
30—		BR INTRET	. . BRANCH TO INTERRUPT RETURN

Fig. 8 - Interrupt routine for 64 x 128 (4 pgs mem).

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.